

**IN THE CLAIMS:**

Please amend claims 8 and 10 as follows:

**LISTING OF CURRENT CLAIMS**

**Claim 8. (Currently Amended)** A method for fabrication of a low temperature polycrystalline silicon thin film transistor comprising the steps of:

- a) selecting a substrate;
- b) forming a buffer oxide on the substrate;
- c) depositing a first amorphous silicon film on the buffer oxide, the first amorphous silicon film being an active layer;
- d) depositing a low-temperature oxide on the first amorphous silicon film;
- e) forming a hard mask being a photoresist on the low temperature oxide;
- f) etching the buffer oxide utilizing a wet isotropic etching process;
- g) depositing a second amorphous silicon film on the active layer;
- h) forming a polysilicon spacer on either side of the active layer by dry etching; and
- i) forming large silicon grain structures in the active layer by annealing and recrystallization of an dog-bone shaped portion of the active layer utilizing one of a high-energy continuous wavelength laser and an excimer laser and recrystallizing the active layer as a polycrystalline silicon,

wherein the low temperature oxide being a stop layer for the first amorphous silicon film during the dry etching process, and a thermal insulating layer and a hard mask for the first amorphous silicon film during laser annealing thereby protecting the polysilicon spacer from removal.

**Claim 9. (Previously Presented)** The method according to claim 8, wherein the polysilicon spacer is selected from a group consisting of polycrystalline silicon film and amorphous silicon film.

**Claim 10. (Currently Amended)** The method according to claim 8, wherein

the polysilicon spacer of the forming step h) is formed on form two opposing sides of the active layer, the active layer is selected from a group consisting of a thin film transistor (TFT) and a silicon-on-insulator metal oxide semiconductor field effect transistor (SOI-MOSFET) in one of a low temperature and a high temperature process.

**Claim 11. (Previously Presented)** The method according to claim 10, wherein in the forming step i) the annealing is performed utilizing a method selected from a group consisting of excimer laser annealing (ELA), solid phase crystallization (SPC), and metal-induced lateral crystallization (MILC), and the polysilicon spacer being formed on opposing sides to the active layer.

**Claim 12. (Previously Presented)** The method according to claim 8, wherein the polysilicon spacer of the forming step h) generates a temperature gradient.

**Claim 13. (Previously Presented)** The method according to claim 8, wherein the etching step (f) is performed before the removal of said hard mask.

**Claim 14. (Previously Presented)** The method according to claim 8, wherein the etching step (f) is performed after the removal of said hard mask.